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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
CHAUDRY, MUJTABA M	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 04/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/838,764	ROOHPARVAR, FRANKIE F.	
	Examiner	Art Unit	
	Mujtaba K. Chaudry	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The corrected or substitute drawings were received on September 13, 2004. These drawings are accepted.

Response to Amendment

Applicant's arguments/amendments with respect to original claims 1-30 filed September 13, 2004 have been fully considered but are not persuasive. The Examiner would like to point out that this action is made final (See MPEP 706.07a).

Applicant contends, "...Nozoe (prior art of record) does not disclose or suggest storing data on the type of defect in the address location..." The Examiner respectfully disagrees. The prior of are record, Nozoe teaches (col. 10) the flash memory comprises an internal voltage generating circuit 31 and a clock generating circuit 32. Based on an external supply voltage Vcc of, say, 3.3V, the internal voltage generating circuit 31 generates voltages needed inside the chip such as a substrate potential, a write voltage, a read voltage and a verify voltage. The clock generating circuit 32 generates a clock (CK) required to control the internal operations. Where necessary, there may be added a defective address register that retains a address of a defective bit, an address comparator that compares a Y address with a defective address, and a redundancy circuit that replaces a selected memory column with a spare memory portion at the time of an address match. The Examiner would like to point out that the type of defect must be known in order to correct it.

The Examiner disagrees with the Applicant and maintains rejections with respect to claims 1-30. All arguments have been considered. It is the Examiner's conclusion that claims 1-30 are not patentably distinct or non-obvious over the prior art of record. See office action:

Claim Rejections - 35 USC § 103

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nozoe et al. (USPN 6351412).

As per claims 1, 8, 12, 17, 20, 24 and 28, Nozoe et al. (herein after: Nozoe) substantially teaches a nonvolatile memory device having an error correcting function, capable of outputting read-out data (uncorrected) while simultaneously generating syndromes. After the syndrome formation, the memory device outputs an error status signal (ERR) and, depending on the presence or absence of an externally supplied request (SC), again outputs read-out data (this time corrected). Nozoe teaches (col. 1-2, lines 1-68) a memory device comprising: a memory array made of a plurality of nonvolatile memory cells arranged in matrix fashion, each of the nonvolatile memory cells being furnished with a control gate and a floating gate and having a

threshold voltage corresponding to data held therein; and an error correcting circuit which receives data read from a plurality of memory cells in the memory array and which corrects any error included in the read-out data: wherein the read-out data are sent in a predetermined block from the memory array to the error correcting circuit while being externally output simultaneously; wherein the error correcting circuit externally outputs, either upon completion of the data output or immediately thereafter, an error status signal indicating whether any error is included in the read-out data; and wherein upon detection of any error in the read-out data of the predetermined block from the memory array, the error correcting circuit corrects the error. Nozoe teaches (cols. 9-10 and Figure 2) a flash memory with the ECC circuit of FIG. 1 mounted on a single semiconductor chip. The memory arrays 20a and 20b are made of nonvolatile memory cells arranged in matrix fashion, each of the cells being constituted by an insulated gate field effect transistor with a floating gate. In the memory arrays, a plurality of word lines and a plurality of bit lines intersect to form a grid pattern. At each point of intersection between a word line and a bit line is a memory cell MC. The control gates of memory cells in a single row are connected to a word line. Alternatively, each word line itself may be arranged to form gate electrodes of memory cells. The drain of each memory cell is connected to the corresponding local bit line which in turn is rendered connectable to a main bit line through a selection OSFET. Word decoders 21a and 21b decode an externally input address signal to bring the corresponding word lines to the selected level in the memory arrays 20a and 20b. Data registers 22a and 22b are connected to the bit lines in the memory arrays 20a and 20b and hold read-out data or data to be written. A sense latch circuit 23 connected to the bit lines in the memory arrays 20 amplifies and retains read-out data. The data amplified by the sense latch circuit 23 can be transferred to

the data registers 22a and 22b through the bit lines in the memory arrays 20a and 20b. Column multiplexers 24a and 24b transmit read-out data from the data registers 22a and 22b to the ECC circuit 10 in a predetermined sequence. A column control circuit 25 comprises an address counter and a decoder. The address counter is updated by an externally supplied serial clock SC, and the decoder decodes the value on the address counter to create control signals for the column multiplexers 24a and 24b. An input/output circuit 26 supplies the word decoders 21a and 21b with an externally input address signal, feeds the error correcting circuit 10 with externally entered data, and outputs corrected data from the error correcting circuit 10 to the external terminal 30 A command decoder 27 decodes a command code given by an external microprocessor or the like A control circuit 28 successively generates control signals for circuits within the memory in order to execute processes specified by externally supplied commands. Effective commands for use by the flash memory of this embodiment include a read command, a write command and an erase command. With this embodiment, externally issued command codes are input through the external terminals 30 which also handle addresses and write data; the input codes are then forwarded to the command decoder 27 via the input/output circuit 26. Because addresses, data and command codes are all input and output through the same external terminals, the number of terminals is far smaller than that in effect if such address, data or command codes. Control signals entered externally into the control circuit 28 include a reset signal RES, a chip selection signal CE, a write control signal WE designating either a read or a write operation, an output control signal OE providing output timing, a serial clock SC, and a command enable signal CDE designating either a command or an address input. Control signals sent by the control circuit 28 to the outside include a ready/busy signal R/B indicating whether

an external command input is acceptable. In addition to the above circuits, the flash memory comprises an internal voltage generating circuit 31 and a clock generating circuit 32. Based on an external supply voltage Vcc of 3.3V, the internal voltage generating circuit 31 generates voltages needed inside the chip such as a substrate potential, a write voltage, a read voltage and a verify voltage. The clock generating circuit 32 generates a clock (CK) required to control the internal operations. The Examiner would like to point out that Nozoe teaches that there may be added a defective address register that retains a location (address) of a defective bit, an address comparator that compares a Y address with a defective address, and a redundancy circuit that replaces a selected memory column with a spare memory portion at the time of an address match. Illustratively, the flash memory of this embodiment includes the two memory arrays 20a and 20b corresponding to the data registers 22a and 22b. Each of the data registers 22a and 22b is arranged to amplify and hold data from memory cells of a single row sharing a word line in the applicable memory array. The read-out data held in the two data registers 22a and 22b are supplemented in increments of four bits with four dummy bits to constitute a 12-bit data structure or the like before the data are transferred to the ECC circuit 10 by the column multiplexers 24a and 24b.

Nozoe does not explicitly teach a state machine to execute an algorithm based on the error code stored in the register as stated in the present application.

However, Nozoe does teach (col. 14) a nonvolatile memory card according to claim 6, wherein the threshold voltage of each of said plurality of memory cells is any one of a first threshold voltage region considered to denote an *erase state* and of a plurality of threshold voltage regions that differ from said first threshold voltage region and which are regarded as

representative of a *write state*. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a state machine with in the methods and apparatus of Nozoe. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have recognized that in order to run various algorithms, for example erase state/write state, a state machine would be convenient in the process.

As per claims 2, 16, 18, 21 and 29, Nozoe teaches, in view of above rejections, (col. 10, lines 24-38) the flash memory to comprise an internal voltage generating circuit 31 and a clock generating circuit 32. Based on an external supply voltage Vcc of, say, 3.3V, the internal voltage generating circuit 31 generates voltages needed inside the chip such as a substrate potential, a write voltage, a read voltage and a verify voltage. The clock generating circuit 32 generates a clock (CK) required to control the internal operations. Where necessary, there may be added a defective address register that retains a location (address) of a defective bit, an address comparator that compares a Y address with a defective address, and a redundancy circuit that replaces a selected memory column with a spare memory portion at the time of an address match.

As per claims 3, 15, 19, 22 and 30, Nozoe teaches, in view of above rejections, (Figure 8) an input/output circuit 26 supplies the word decoders 21a and 21b with an externally input address signal, feeds the error correcting circuit 10 with externally entered data, and outputs corrected data from the error correcting circuit 10 to the external terminal 30 A command decoder 27 decodes a command code given by an external microprocessor or the like A control circuit 28 successively generates control signals for circuits within the memory in order

to execute processes specified by externally supplied commands. Effective commands for use by the flash memory of this embodiment include a read command, a write command and an erase command. Nozoe also teaches a nonvolatile memory card according to claim 6, wherein the threshold voltage of each of said plurality of memory cells is any one of a first threshold voltage region considered to denote an erase state and of a plurality of threshold voltage regions which differ from said first threshold voltage region and which are regarded as representative of a write state.

As per claims 4-7, 9-11, 13-14, 23 and 25-27, Nozoe teaches, in view of above rejections, (Figures 1-2) a flash memory embodying a ECC circuit 10 that comprises: a syndrome and correct code forming circuit 11 which successively receives one sector (e.g., 2,106 bytes) of data from a memory array and forms syndromes accordingly; an error judging circuit 12 for judging whether any error is included in the read-out data by checking to see if all formed syndromes are zeros; a correction location information generating circuit 13 for generating location information about faulty bits based on the formed syndromes; a coincidence detecting circuit 14 for checking to see which byte contains an error through comparison of three bytes (1 byte equals 12 bits) of data coming from the correction location information generating circuit 13; an error correcting circuit 15 for correcting any read error based on the generated correction located information; and a gate 16 for enabling and disabling the output of the correction location information generating circuit 13 to the error correcting circuit 15 in accordance with a detection signal from the coincidence detecting circuit 14. In Figure 2, Nozoe teaches a block diagram of the flash memory with the ECC circuit of FIG. 1 mounted on a single semiconductor chip. The memory arrays 20a and 20b are made of nonvolatile memory cells arranged in matrix

fashion, each of the cells being constituted by an insulated gate field effect transistor with a floating gate. In the memory arrays, a plurality of word lines and a plurality of bit lines intersect to form a grid pattern. At each point of intersection between a word line and a bit line is a memory cell MC. The control gates of memory cells in a single row are connected to a word line. Alternatively, each word line itself may be arranged to form gate electrodes of memory cells. The drain of each memory cell is connected to the corresponding local bit line which in turn is rendered connectable to a main bit line through a selection MOSFET. Furthermore, Nozoe teaches the flash memory to have two memory arrays 20a and 20b corresponding to the data registers 22a and 22b. Each of the data registers 22a and 22b is arranged to amplify and hold data from memory cells of a single row sharing a word line in the applicable memory array. The read-out data held in the two data registers 22a and 22b are supplemented in increments of four bits with four dummy bits to constitute a 12-bit data structure or the like before the data are transferred to the ECC circuit 10 by the column multiplexers 24a and 24b. a memory device comprising: a memory array made of a plurality of nonvolatile memory cells arranged in matrix fashion, each of the nonvolatile memory cells being furnished with a control gate and a floating gate and having a threshold voltage corresponding to data held therein; and an error correcting circuit which receives data read from a plurality of memory cells in the memory array and which corrects any error included in the read-out data: wherein the read-out data are sent in a predetermined block from the memory array to the error correcting circuit while being externally output simultaneously; wherein the error correcting circuit externally outputs, either upon completion of the data output or immediately thereafter, an error status signal indicating whether any error is included in

the read-out data; and wherein upon detection of any error in the read-out data of the predetermined block from the memory array, the error correcting circuit corrects the error.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiries concerning this communication should be directed to the examiner, Mujtaba Chaudry who may be reached at 571-272-3817. The examiner may normally be reached Mon – Thur 6:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Albert DeCady at 571-272-3819.

Mujtaba Chaudry
Art Unit 2133
April 20, 2005

GUY LAMARRE
PRIMARY EXAMINER